REMARKS

There is no Office Action outstanding with respect to this application. The following comments are provided in response to the Office Action issued 16 February 2001 in the parent application, U.S. Serial No. 09/621,012.

In the parent application, the phrase "outside the range of voltages used to represent logic signals" was found to be unclear. That phrase appears, for example, in claims 138, 142, 143, 147, 152, 160 and 163. That language refers to a voltage that is not one of the voltages used to represent logic signals. It is respectfully submitted that the language appearing in the claims is clear and unambiguous to a person of ordinary skill in the art. For example, see U.S. Patent No. 5, 724,289 to Watanabe, col. 8, lines 59 through 69 which provide:

> In FIG. 4, if a test voltage higher than a usually used voltage, VHH, is applied to any one of the test node terminals TEST 1 through TEST n, e.g., TEST i, then the voltage detector 210 in the automated count setter 11A detects the voltage higher than the usually used one VCC being applied to the terminal TEST i.

If the Examiner is of the opinion that the language appearing in the claims still needs revision, applicants' attorney is open to suggestions.

Certain of the claims of the parent application, for example, claims 71, 126 and 135, were rejected in view of U.S. Patent No. 5,384,784 to Mori, et al. It is respectfully submitted that the subject matter of those claims is patentable over Mori, et al. for the following reasons.

In claims 71, 126 and 135, data is written to a first seed row or a first seed group of memory elements. The data in the first seed row or the first seed group is then latched and the latched data is used to write other memory elements. The Examiner has pointed to

nothing in Mori, et al which discloses or suggests the use of a "seed row" or a "seed group" from which the other memory elements are written. In particular, the prior art illustrated in FIG. 41 of Mori, et al illustrates a latch 110 for each pair of bit lines. In contrast, and as discussed more fully on pages 200 through 204 of the instant application, once the seed row is written, the present invention allows the data stored in the seed row to be quickly duplicated into the remaining rows. More specifically, by firing the appropriate word line, the data stored in the seed row is placed on the digit lines. Once the data is on the digit lines, the data is latched by the sense amps. Thereafter, the latched data may be stored in any row by firing the appropriate word line to connect that row to the digit lines. Such a scheme is not disclosed or suggested in Mori, et al.

Certain of the other claims of the parent application, such as claims 138, 142, 143 and 160 were rejected as being anticipated by Roohparvar, U.S. Patent No. 5,526,364. It is respectfully submitted that Roohparvar does not anticipate those claims. Claim 138 recites the step of inputting to a solid state device a series of control signals, while claims 142 and 143 recite the step of enabling a detector, and claim 160 recites an enable circuit for determining if, for example, an elevated voltage is applied "under predetermined conditions." As discussed more fully in the specification of the instant application at pages 143 and 144, to prevent inadvertent access to the test mode, a certain combination of control signals must be present before the solid state device can accept a voltage outside the range of normal voltages as an indication that a test mode is desired. In Roohparvar, as well as the other references, there is nothing cited to indicate that a certain sequence of signals or a certain step, such as enabling a detector, is required before the solid state device accepts an elevated voltage as an indication of a desire to enter the test mode.

Claim 147 of the parent application was rejected under 35 U.S.C.§102(b) over Mori et at. Claim 147 recites a first step of "applying to the device a voltage outside the range of voltages . . . and while said voltage is being applied" a second step of "sequentially inputting at least two addresses to said device." The first address contains information used to confirm the presence of the voltage outside the range of voltages and the second address contains information used to place the device into a test mode. The purpose of sequentially inputting two addresses is to provide insurance that the device is not inadvertently placed in a test mode. As set forth in claim 147 after, for example, an over voltage is applied to the device, the first address is used to confirm the presence of the voltage and thus confirms that the device is to be placed in a test mode, and the second address places the device in a desired test mode. There is no such sequential input of address information to the device of Mori et al, with the first address being used to confirm that the device is to be placed in the test mode and the second address used to place the device in a desired test mode.

Claim 152 of the parent application was rejected in view of U.S. Patent No. 5,724,289 to Watanabe. Claim 152 recites, among other limitations, "applying a specific combination of control signals to enable the receipt of a test enable key." The next step recited in claim 152 is "applying said specific combination of control signals to enable the receipt of at least one test mode key," followed by "decoding the test mode key to place the device in a test mode." It is respectfully submitted that the device in Watanabe is placed in a test mode by simply applying a voltage higher than a usually used voltage to one of the terminals Test 1 through Test 4. See column 8, lines 59 - 69 and column 10, lines 3 - 8. The method set forth in claim 152 is designed to prevent a solid state device from inadvertently entering a test mode through the chance application of an elevated voltage on

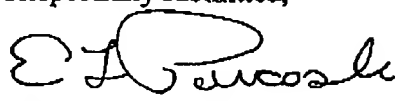
a particular input pin. In the claimed invention, there must first be a specific combination of control signals before the test enable key can even be received. After the test enable key has been received, the key is used to verify that a test mode is desired. After those steps, a specific combination of control signals must again be applied to enable the receipt of a test mode key, which is decoded to finally place the device in the desired test mode. That is a substantially different method than the method set forth in Watanabe. It is respectfully submitted that Watanabe neither discloses nor anticipates the method set forth in claim 152.

Finally, claim 70 of the parent application was rejected under 35 U.S.C. §103(a) over Watanabe in view of Roohparvar. As discussed above in conjunction with claim 71, claim 70 sets forth the writing of test data into a first seed row of memory elements. The test data from the first seed row is then latched, and used to write test data into subsequent groups. It is respectfully submitted that Watanabe does not disclose or suggest the use of a seed row, and neither does Roohparvar. Accordingly, the combination of those references cannot render obvious the method as set forth in claim 70.

Claims 166 – 207 are dependent claims. No new matter has been added.

Claims 70, 71, 100, 120, 126, 135, 136, 138-143, 147, 152, 160-207 are believed to be in condition for allowance over the art cited in the application to date. An early Office Action on the merits is respectfully requested.

Respectfully submitted,



Edward L. Pencoske
Reg. No. 29,688
THORP REED & ARMSTRONG, LLP
One Oxford Centre, 14th Floor
301 Grant Street
Pittsburgh, PA 15219-1425
(412) 394-7789
Attorney for Applicants

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	)	
		)	**Examiner:**
Serial No.:	09/899,977	)	
		)	**Art Unit:** 2818
Filed:	07/06/2001	)	

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

Complete Clean Set of Pending Claims

70. (Once Amended) A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements, and an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

71.(Once Amended) A method of testing a plurality of memory elements organized in a plurality of rows, comprising the steps of:

writing test data into a first seed row of memory elements;

latching the test data from the first seed row of memory elements in response to a first external signal;

writing the latched test data into subsequent groups of memory elements in response to a second external signal;

reading the test data from the subsequent groups of memory elements; and

comparing the test data read from the subsequent groups of memory elements with the test data written to the first seed row of memory elements.

100. (Once Amended) A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral device; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory cells, and an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory cells.

120. (Once Amended) A combination for use in a memory having an array of memory elements, said combination comprising:

test mode logic for determining whether the memory is in a test mode;

a latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements; and

an enable circuit responsive to a second external signal when the memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

126. (Once Amended) A method of writing to a plurality of memory elements, comprising the steps of:

writing known data into a first seed group of memory elements;

latching the data from the first seed group of memory elements in response to a first external signal; and

writing the latched data into a second group of memory elements in response to a second external signal.

135. (Once Amended) A method of testing a portion of a memory array having a plurality of memory elements formed in a plurality of rows, and wherein said array is arranged in a plurality of memory blocks, said method comprising the steps of:

selecting a memory block for testing:

writing test data into a first seed row of memory elements in the selected memory block;

latching the test data from the first seed row of memory elements in response to a first external signal;

writing the latched test data into subsequent pluralities of rows of memory elements in response to a second external signal;

reading the test data from the memory block; and

comparing the test data read from the memory block with the test data written into the first seed row.

136. The method of claim 135 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

138. (Once Amended) A method, comprising:

inputting to a solid state device a series of control signals;

inputting to the device a voltage outside the range of voltages used to represent logic signals;

inputting at least one address to the device; and

decoding the address to ascertain test mode information.

139. The method of claim 138 wherein the step of inputting the voltage includes the step of inputting a voltage higher than the highest voltage used to represent logic signals in the device.

140. The method of claim 138 wherein said step of inputting at least one address to the device is performed while the step of inputting a voltage is being performed.

141. The method of claim 140 additionally comprising the step of decoding the address information to ascertain if the test mode information includes instructions to test for the presence of the voltage outside the range of voltages used to represent logic signals in the device.

142. A method of placing a solid state device into a mode in which it is capable of receiving test mode information, comprising:

inputting to the device a voltage outside the range of voltages used to represent logic signals;

enabling a detector; and

confirming with said detector the presence of the voltage outside the range of voltages used to represent logic signals.

143. (Once Amended) A method of inputting test mode information to a solid state device, comprising:

enabling a detector;

inputting to the device a voltage outside the range of voltages used to represent logic signals;

confirming the presence of the voltage outside the range of voltages used to represent logic signals; and

inputting to the device at least one address containing test mode information.

147. (Once Amended) A method of placing a solid state device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

sequentially inputting at least two addresses to said device, said first address containing information used to confirm the presence of said voltage outside the range of voltages used to represent logic signals, and said second address containing information used to place the device into a test mode.

152. A method of placing a solid state memory device into a test mode, comprising:

applying to the device a voltage outside the range of voltages used to represent logic signals, and while said voltage is being applied;

applying a specific combination of control signals to enable the receipt of a test enable key;

verifying the test enable key and confirming the presence of the applied voltage;

applying said specific combination of control signals to enable the receipt of at least one test mode key; and

decoding the test mode key to place the device in a test mode.

160. A test logic circuit for a solid state memory device, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit.

161. The test logic circuit of claim 160 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

162. The test logic circuit of claim 160 additionally comprising a circuit for inhibiting said solid state memory device from normal operations when the device is in a test mode.

163. A solid state memory device, comprising:

a plurality of memory cells;

a plurality of peripheral devices for writing information into and reading information out of said memory cells; and

a test logic circuit, comprising:

a test mode enable circuit for determining if a voltage outside the range of voltages used to represent logic levels is being applied to the memory device under predetermined conditions; and

a circuit for receiving and decoding test mode keys in response to said test mode enable circuit;

said memory device further comprising circuits, responsive to said decoded test mode keys, for performing tests on at least one of said memory cells and peripheral devices.

164. The memory device of claim 163 wherein said test mode enable circuit includes logic for receiving a row address strobe signal (RAS), a write column address strobe before RAS signal, the applied voltage, and certain address information on column address lines and for producing therefrom a latch signal.

165. The memory device of claim 164 additionally comprising a test mode reset circuit for resetting said circuit for receiving and decoding test mode keys.

166. The memory of claim 70 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

167. The memory of claim 166 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array

blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

168. The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

169. The memory of claim 70 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

170. The memory of claim 70 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

171. The memory of claim 70 wherein said memory provides at least 256 meg of storage.

172. The memory of claim 171 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

173. The method of claim 71 wherein the first external signal is a row address strobe signal and the second external signal is a column address strobe signal.

174. The method of claim 173 wherein writing into subsequent groups of memory elements includes writing into multiple rows in response to each cycle of the column address strobe signal.

175. The system of claim 100 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

176. The system of claim 175 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

177. The system of claim 100 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

178. The system of claim 177 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

179. The system of claim 178 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage

regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

180. The system of claim 179 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

181. The system of claim 179 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

182. The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

183. The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

184. The system of claim 100 wherein said memory provides at least 256 meg of storage.

185. The system of claim 184 wherein said array provides more than 256 meg of storage. said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

186. The combination of claim 120 wherein said first external signal includes a row address strobe signal.

187. The combination of claim 120 wherein said second external signal includes a column address strobe signal.

188. The method of claim 126 wherein the first external signal is a row address signal and the second external signal is a column address strobe signal.

189. The method of claim 188 additionally comprising the step of writing into subsequent groups of memory elements in response to each cycle of the column addresses strobe signal.

190. The method of claim 126 wherein said step of latching the data includes the step of connecting each memory element in the first seed group to one of a plurality of sense amps.

191. The method of claim 190 wherein said step of connecting each memory element includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in said first seed group to one of the sense amps.

192. The method of claim 191 wherein said step of writing the latched data into a second group of memory elements includes the step of connecting each memory element in the second group to one of the sense amps.

193. The method of claim 192 wherein said step of connecting each memory element in the second group includes the step of biasing a plurality of isolation transistors into conductive states to connect each memory element in the second group to one of the sense amps.

194. The method of claim 142 wherein the receipt of the sequence of a write enable signal, column address strobe signal and a row address strobe signal enables the detector.

195. The method of claim 143 wherein said step of enabling a detector is performed by the step of inputting a sequence of control signals.

196. The method of claim 195 wherein said sequence of control signals includes a write enable signal, column address strobe signal and row address strobe signal.

197. The method of claim 143 wherein said step of inputting at least one address to the device is performed while said step of inputting a voltage is performed.

198. The method of claim 143 wherein said step of inputting at least one address includes the step of inputting a first address for confirming that the device is to be in a test mode and inputting a second address for specifying a test mode.

199. The method of claim 147 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

200. The method of claim 147 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

201. The method of claim 147 additionally comprising the step of inputting an address containing information to take the device out of a test mode.

202. The method of claim 152 wherein the step of applying a voltage includes the step of applying a voltage higher than the highest voltage used to represent logic signals in the device.

203. The method of claim 152 additionally comprising the step of inhibiting the device from normal operation while said step of applying a voltage is performed.

204. The method of claim 152 additionally comprising the step of ending the application of a voltage outside the range of voltages used to represent logic signals to take the device out of a test mode.

205. The method of claim 152 additionally comprising the step of inputting a clear test mode key to take the device out of a test mode.

206. The method of claim 152 wherein said test mode keys are received as address information on column address lines.

207. The method of claim 152 additionally comprising the steps of performing the test specified by the test mode key and outputting the test results.